Kodak

DEVICE
PERFORMANCE
SPECIFICATION

KAF -0402E/ME

768 (H) x 512 (V)
Enhanced Response Full-Frame
CCD

January 29, 2003
Revision 1

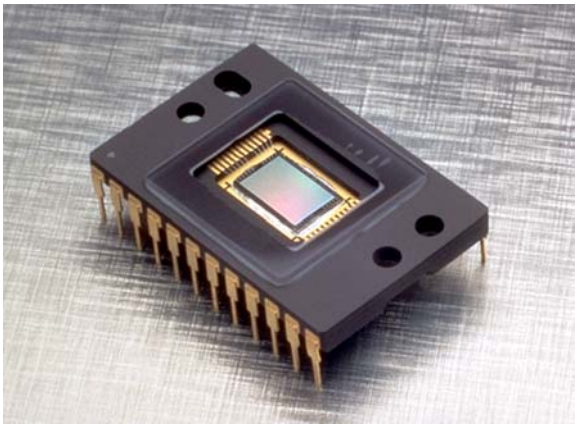
www.kodak.com/go/imagers 585-722-4385 Email: imagers@kodak.com

TABLE OF CONTENTS

TABLE OF FIGURES

SUMMARY SPECIFICATION

KODAK KAF-0402E/ME Image Sensor 768 (H) x 512 (V) Enhanced Response Full-Frame CCD



Description

The KAF-0402E/ME is a high performance monochrome area CCD (charge-coupled device) image sensor with 768H x 512V photoactive pixels. It is designed for a wide range of image sensing applications in the 350 nm to 1000 nm wavelength band. Typical applications include military, scientific, and industrial imaging. Low dark current and good charge capacity result in 76 dB dynamic range at room temperature.

The sensor is built with a true two-phase CCD technology employing a transparent gate. This technology simplifies the support circuits that drive the sensor, reduces the dark current without compromising charge capacity, and significantly increases to optical response compared to traditional front illuminated full frame sensors.

The ME configuration adds micro lenses to the surface of the CCD sensor. These lenses focus the majority of the light through the transparent gate, increasing the optical response further.

The photoactive area is 6.91mm x 4.6 mm. The imager is housed in a 24 -pin, 0.805" wide, dual in line package with 0.100" pin spacing.

Parameter	Value
Architecture	Full-Frame CCD; Enhanced Response
Total Number of Pixels	784 (H) x 520 (V)
Number of Active Pixels	768 (H) x 512 (V) = approx. 0.4M
Pixel Size	9.0µm (H) x 9.,0µm (V)
Imager Size	6.91(H)mm x 4.6(V)mm
Die Size	8.4mm (H) x 5.5mm (V)
Aspect Ratio	3:2
Saturation Signal	100,000 electrons
Quantum Efficiency	Peak with Microlens: 77% Peak without Microlens: 65% 400 nm with Microlens: 45% 400nm without Microlens: 30%
Output Sensitivity	10 µV/e
Read Noise	15 electrons
Dark Current	<10pA/cm^2 @ 25°C
Dark Current Doubling Temperature	6.3°C
Dynamic Range	76 dB
Charge Transfer Efficiency	>0.99999
Blooming Suppression	None
Maximum Data Rate	10 MHz

DEVICE DESCRIPTION

Architecture

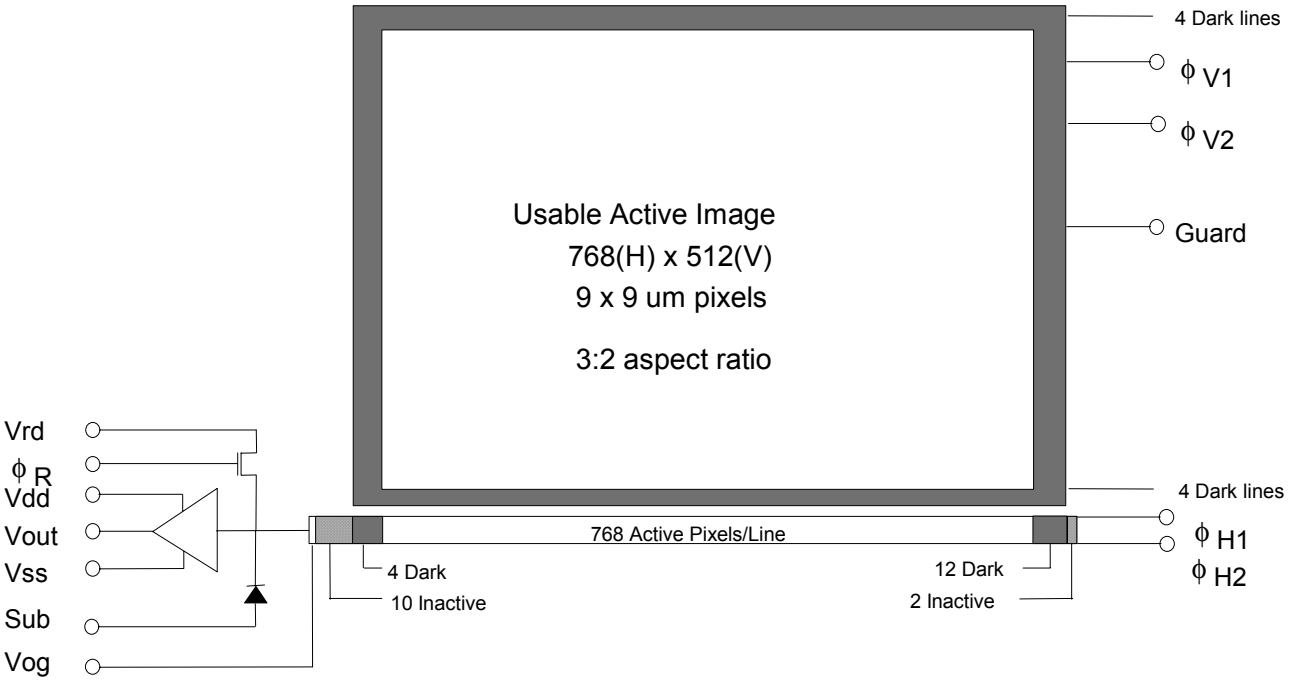


Figure 1 Functional block diagram

The sensor consists of 784 parallel (vertical) CCD shift registers each 520 elements long. These registers act as both the photosensitive elements and as the transport circuits that allow the image to be sequentially read out of the sensor. The parallel (vertical) CCD registers transfer the image one line at a time into a single 796-element (horizontal) CCD shift register. The horizontal register transfers the charge to a single output amplifier. The output amplifier is a two-stage source follower that converts the photo-generated charge to a voltage for each pixel.

Micro lenses

Micro lenses are formed along each row. They are effectively half of a cylinder centered on the transparent gates, extending continuously in the row direction. They act to direct the photons away from the polysilicon gate and through the transparent gate. This increases the response, especially at the shorter wavelengths (< 600 nm).

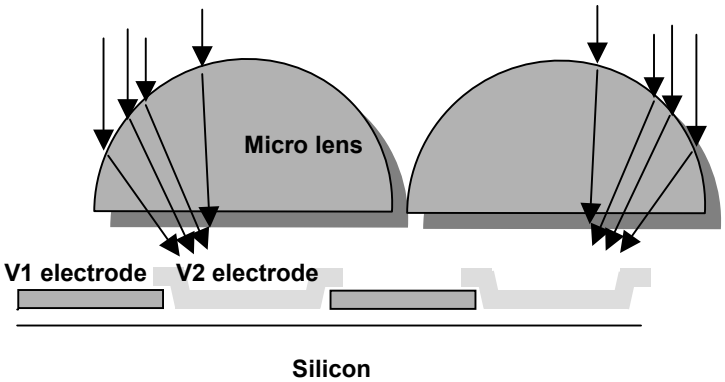


Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the sensor. These photon induced electrons are collected locally by the formation of potential wells at each photogate or pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons will leak into the adjacent pixels within the same column. This is termed blooming. During the integration period, the ϕV1 and ϕV2 register clocks are held at a constant (low) level. See Figure 7 Timing diagrams.

Charge Transport

Referring again to “Figure 7 Timing diagrams”, the integrated charge from each photogate is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCD to the horizontal CCD register using the ϕV1 and ϕV2 register clocks. The horizontal CCD is presented a new line on the falling edge of ϕV2 while ϕH1 is held high. The horizontal CCD then transports each line, pixel by pixel, to the output structure by alternately clocking the ϕH1 and ϕH2 pins in a complementary fashion. On each falling edge of ϕH2 a new charge packet is transferred onto a floating diffusion and sensed by the output amplifier.

Output Structure

Charge presented to the floating diffusion is converted into a voltage and current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the floating diffusion. Once the signal has been sampled by the system electronics, the reset gate (ϕR) is clocked to remove the signal and the floating diffusion is reset to the potential applied by Vrd. (see Figure 3 Output schematic). More signal at the floating diffusion reduces the voltage seen at the output pin. In order to activate the output structure, an off-chip load must be added to the Vout pin of the device such as shown in Fig 4.

Dark Reference Pixels

There are 4 light shielded pixels at the beginning of each line, and 12 at the end. There are 4 dark lines at the start of every frame and 4 dark lines at the end of each frame. Under normal circumstances, these pixels do not respond to light. However, dark reference pixels in close proximity to an active pixel can scavenge signal depending on light intensity and wavelength and therefore will not represent the true dark signal.

Dummy Pixels

Within the horizontal shift register are 10 leading additional pixels that are not associated with a column of pixels within the vertical register. These pixels contain only horizontal shift register dark current signal and do not respond to light. A few leading dummy pixels may scavenge false signal depending on operating conditions. There are two more dummy pixels at the end of each line.

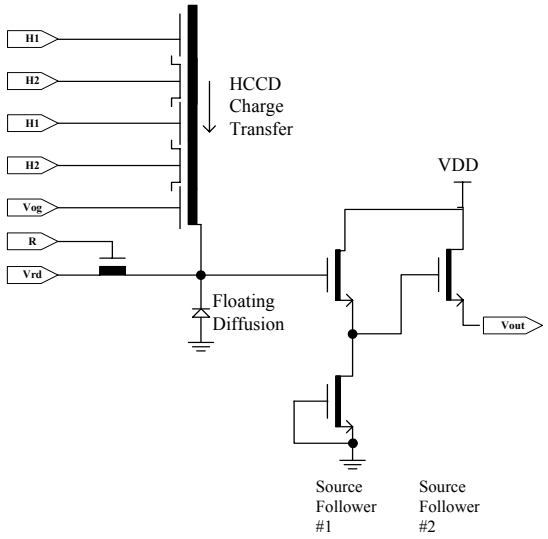


Figure 3 Output schematic

Physical Description

Pin Description

Pin	Symbol	Description	Pin	Symbol	Description
1	VOG	Output Gate	13	N/C	No connection (open pin)
2	VOUT	Video Output	11,14	VSUB	Substrate (Ground)
3	VDD	Amplifier Supply	15, 16, 21,22	ϕV1	Vertical CCD Clock - Phase 1
4	VRD	Reset Drain	17, 18, 19,20	ϕV2	Vertical CCD Clock - Phase 2
5	ϕR	Reset Clock	23	Guard	Guard Ring
6	VSS	Amplifier Supply Return	24	N/C	No Connection (open pin)
7	ϕH1	Horizontal CCD Clock - Phase 1			
8	ϕH2	Horizontal CCD Clock - Phase 2			
9, 10, 12	N/C	No connection (open pin)			

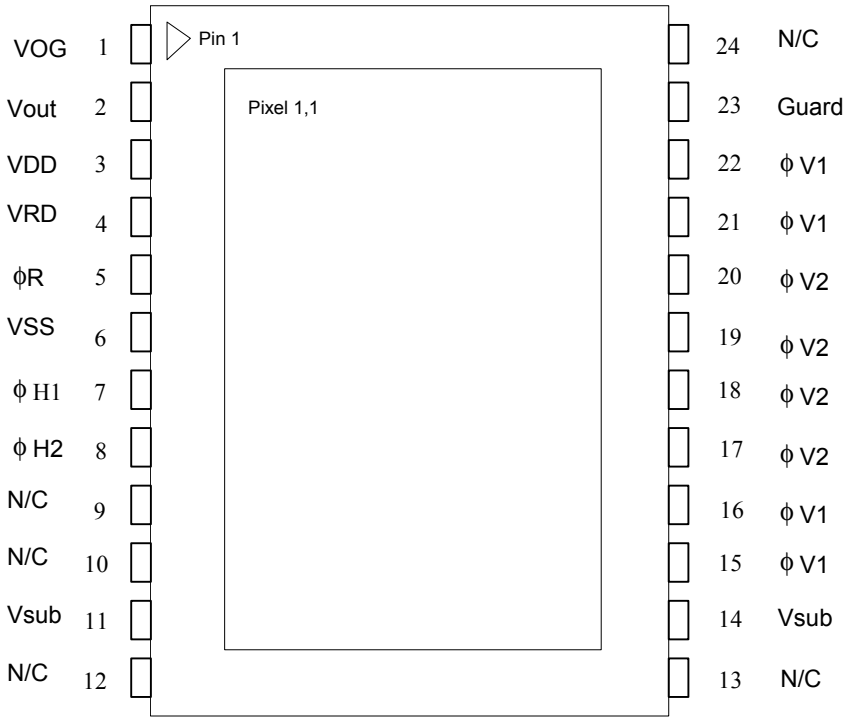


Figure 4 Package pin designation

Performance

Electro Optical Specifications

All values measured at 25°C, and nominal operating conditions. These parameters exclude defective pixels.

Description	Symbol	Min	Nom	Max	Unit	Notes
Saturation Signal **Vertical CCD capacity** **Horizontal CCD capacity** **Output Node capacity**	Nsat	 85000 170000 190000	 100000 200000 220000	 240000	electrons / pixel	 1
Quantum Efficiency (see Figure 5 Spectral response)						
Photoresponse Non-Linearity	PRNL		1.0	2.0	%	2
Photoresponse Non-Uniformity	PRNU		0.8		%	3
Dark Signal	Jdark		15 6	30 10	electrons / pixel / sec pA/cm^2	4
Dark Signal Doubling Temperature			6.3	7	°C	
Dark Signal Non-Uniformity	DSNU		15	30	electrons / pixel / sec	5
Dynamic Range	DR	72	76		dB	6
Charge Transfer Efficiency	CTE	0.99997	0.99999			
Output Amplifier DC Offset	Vodc	Vrd	Vrd + 0.5	Vrd + 1.0	V	
Output Amplifier Sensitivity	Vout/Ne~	9	10		uV/e~	
Output Amplifier output Impedance	Zout	180	200	220	Ohms	
Noise Floor	ne~		15	20	electrons	7

Notes:

1. For pixel binning applications, electron capacity up to 330000 can be achieved with modified CCD inputs. Each sensor may have to be optimized individually for these applications. Some performance parameters may be compromised to achieve the largest signals.
2. Worst case deviation from straight line fit, between 2% and 90% of Vsat.
3. One Sigma deviation of a 128x128 sample when CCD illuminated uniformly at half of saturation.
4. Average of all pixels with no illumination at 25 °C..
5. Average dark signal of any of 11 x 8 blocks within the sensor (each block is 128 x 128 pixels).
6. 20log (Nsat / ne~) at nominal operating frequency and 25 °C
7. Noise floor is specified at the nominal pixel frequency and excludes any dark or pattern noises. It is dominated by the output amplifier power spectrum with a bandwidth = 5 * pixel rate.

Spectral Response

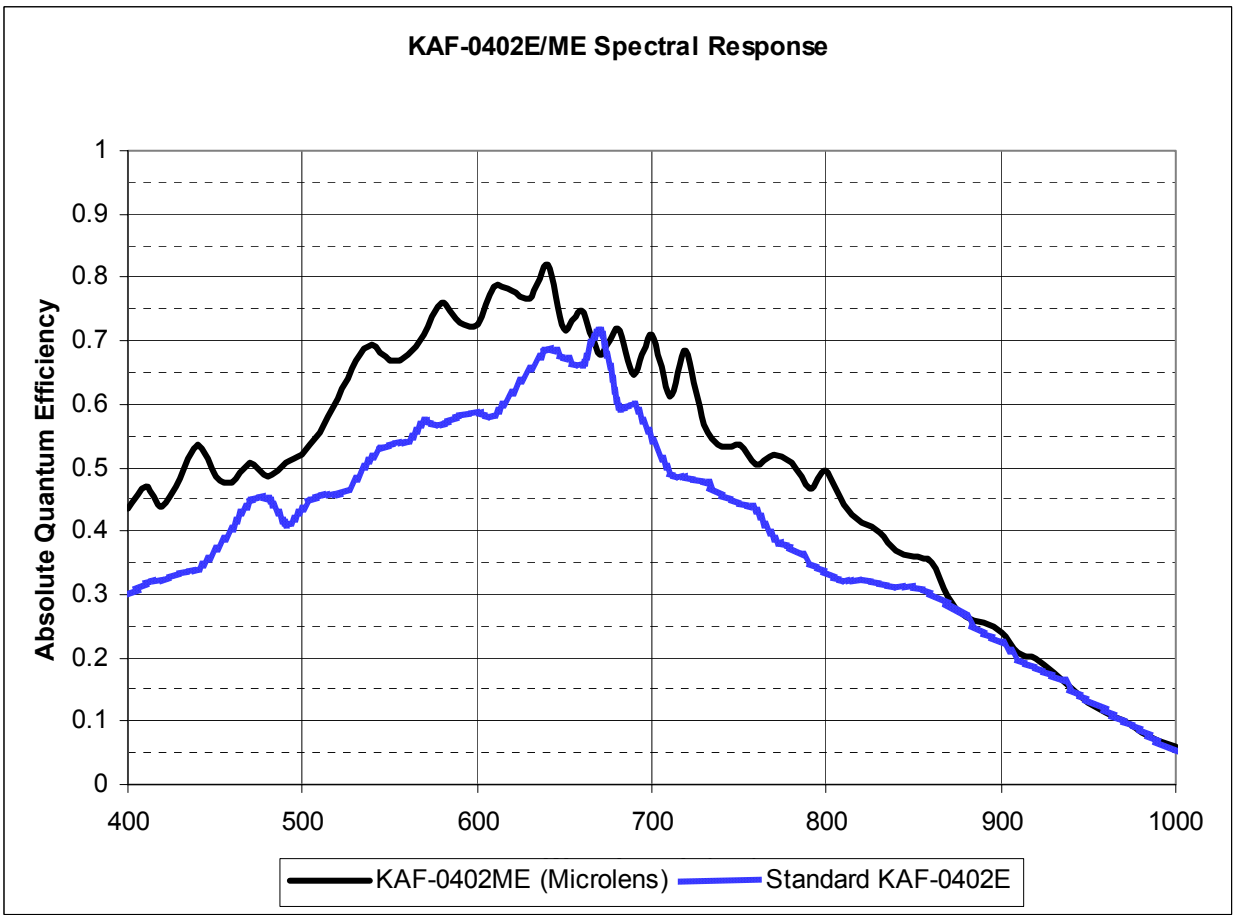
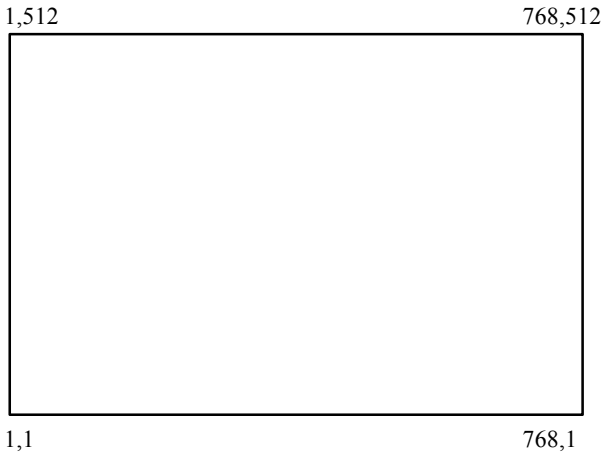


Figure 5 Spectral response

Cosmetic Specification

Defect tests performed at T=25°C

Grade	Point Defects	Cluster Defects	Column
C1	≤5	0	0
C2	≤10	≤4	0



Cosmetic Definitions

Point Defect	DARK: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation, OR BRIGHT: A Pixel with dark current > 5000 e/pixel/sec at 25C.
Cluster Defect	A grouping of not more than 5 adjacent point defects.
Column Defect	1) A grouping of >5 contiguous point defects along a single column. 2) A column containing a pixel with dark current > 12,000e/pixel/sec (bright column). 3) A column that does not meet the minimum vertical CCD charge capacity (low charge capacity column). 4) A column which loses more than 250 e under 2Ke illumination (trap defect).
Neighboring pixels	The surrounding 128 x 128 pixels or ±64 columns/rows.
Defect Separation	Column and cluster defects are separated by no less than two (2) pixels in any direction (excluding single pixel defects).

Operation

Absolute Maximum Ratings

Description	Symbol	Min	Max	Unit	Notes
Diode Pin Voltages	Vdiode	0	20	V	1,2
Gate Pin Voltages	Vgate1	-16	16	V	1,3,6
Output Bias Current	Iout		-10	mA	4
Output Load Capacitance	Cload		15	pF	4
Storage Temperature	T		100	^{o}C	
Humidity	RH	5	90	%	5

Notes:

1. Referenced to pin Vsub or between each pin in this group.
2. Includes pins: Vrd, Vdd, Vss, Vout.
3. Includes pins: ϕV1, ϕV2, ϕH1, ϕH2, Vog, Vlg. ϕR.
4. Avoid shorting output pins to ground or any low impedance source during operation.
5. T=25°C. Excessive humidity will degrade MTTF.
6. This sensor contains gate protection circuits to provide some protection against ESD events. The circuits will turn on when greater than 16 volts appears between any two gate pins. Permanent damage can result if excessive current is allowed to flow under these conditions.

CAUTION: This device contains limited protection against Electrostatic Discharge (ESD). Devices should be handled in accordance with strict ESD procedures for Class 0 devices (JESD22 Human Body Model) or Class A (Machine Model). Refer to Application Note MTD/PS-0224, "Electrostatic Discharge Control"

DC Operating Conditions

Description	Symbol	Min	Nom	Max	Unit	Max DC Current (mA)	Notes
Reset Drain	Vrd	10	11.0	11.5	V	0.01	
Output Amplifier Return	Vss	1.5	2.0	2.5	V	-0.5	
Output Amplifier Supply	Vdd	14.75	15	15.5	V	Iout	
Substrate	Vsub	0	0	0	V	0.01	
Output Gate	Vog	3.75	4	5	V	0.01	
Gueard Ring	Vlg	8.0	9.0	12.0	V	0.01	
Video Output Current	Iout		-5	-10	mA	-	1

Notes:

1. An output load sink must be applied to Vout to activate output amplifier - see Figure below.

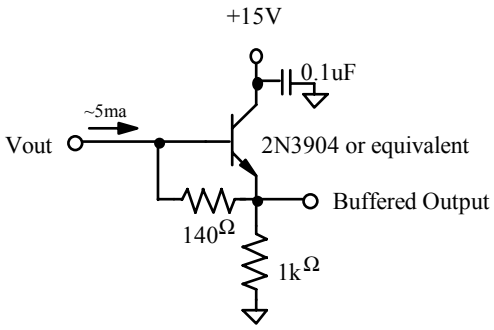


Figure 6 Example Output Structure Load Diagram

AC Operating Condition

Description	Symbol	Level	Min	Nom	Max	Unit	Effective Capacitance
Vertical CCD Clock - Phase 1	ϕV1	Low High	-10.5 -0.5	-10.0 0	-9.5 1.0	V V	6 nF (all ØV1 pins)
Vertical CCD Clock - Phase 2	ϕV2	Low High	-10.5 -0.5	-10.0 0	-9.5 1.0	V V	6 nF (all ØV2 pins)
Horizontal CCD Clock - Phase 1	ϕH1	Low Amplitude	-4.5 9.5	-4.0 10.0	-3.5 10.5	V V	50pF
Horizontal CCD Clock - Phase 2	ϕH2	Low Amplitude	-4.5 9.5	-4.0 10.0	-3.5 10.5	V V	50pF
Reset Clock	ϕR	Low Amplitude	-3.0 5.0	-2.0 6.0	-1.75 7.0	V V	5pF

Notes:
1. All pins draw less than 10uA DC current.
2. Capacitance values relative to VSUB.

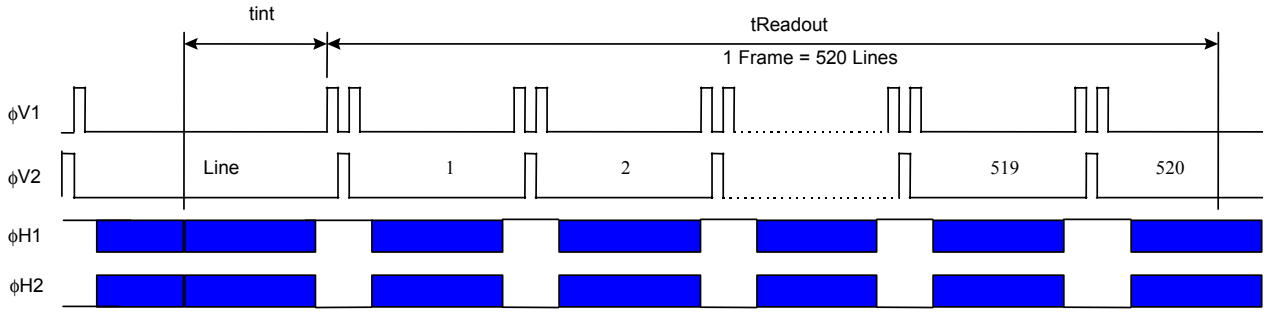
AC Timing Conditions

Description	Symbol	Min	Nom	Max	Unit	Notes
ϕH1, ϕH2 Clock Frequency	f_H		4	10	MHz	1, 2, 3
Pixel Period (1 Count)	t_e	100	250		ns	
ϕH1, ϕH2 Setup Time	$t_{\phi HS}$	0.5	1		us	
ϕV1, ϕV2 Clock Pulse Width	$t_{\phi V}$	1.5	2		us	2
Reset Clock Pulse Width	$t_{\phi R}$	10	20		ns	4
Readout Time	$t_{readout}$	43.7	107		ms	5
Integration Time	t_{int}					6
Line Time	t_{line}	84.1	206		us	7

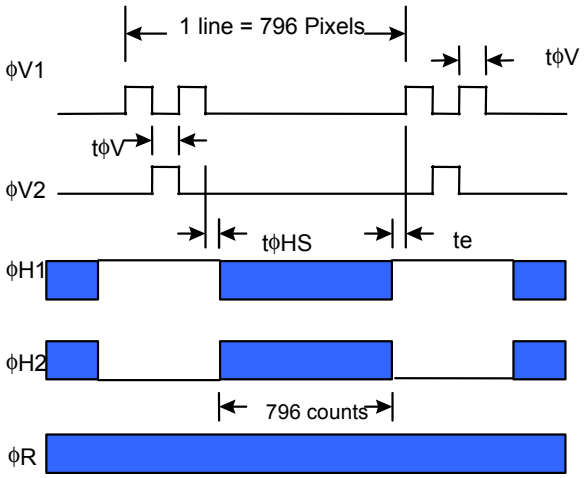
Notes:
1. 50% duty cycle values.
2. CTE may degrade above the nominal frequency.
3. Rise and fall times (10/90% levels) should be limited to 5-10% of clock period. Cross-over of register clocks should be between 40-60% of amplitude.
4. ϕR should be clocked continuously.
5. $t_{readout} = (520*t_{line})$
6. Integration time is user specified. Longer integration times will degrade noise performance due to dark signal fixed pattern and shot noise.
7. $t_{line} = (3*t_{\phi v}) + t_{\phi HS} + (796*t_e) + t_e$

Timing diagrams

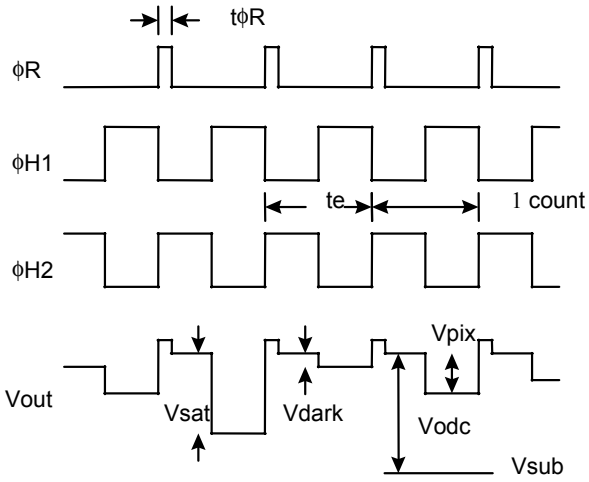
Frame Timing



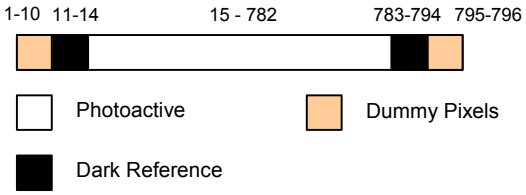
Line Timing



Pixel Timing



Line Content



Vsat	Saturated pixel video output
Vdark	Video output signal in no light situation, not zero due to
Vpix	Pixel video output signal level, more electrons =more
Vodc	Video level offset with respect to
Vsub	Analog

* See Image Aquisition section

Figure 7 Timing diagrams

QUALITY ASSURANCE AND RELIABILITY

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer.

Liability of the Customer: Damage from mechanical (scratches or breakage), electrostatic discharge (ESD), or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning for Image Sensors, for further information.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224, Electrostatic Discharge Control, for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

ORDERING INFORMATION

Available Part Configurations

Type	Description	Glass Configuration
KAF-0402E	Monochrome	
KAF-0402ME	Monochrome, microlens	

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

Physical Description

Package Drawing

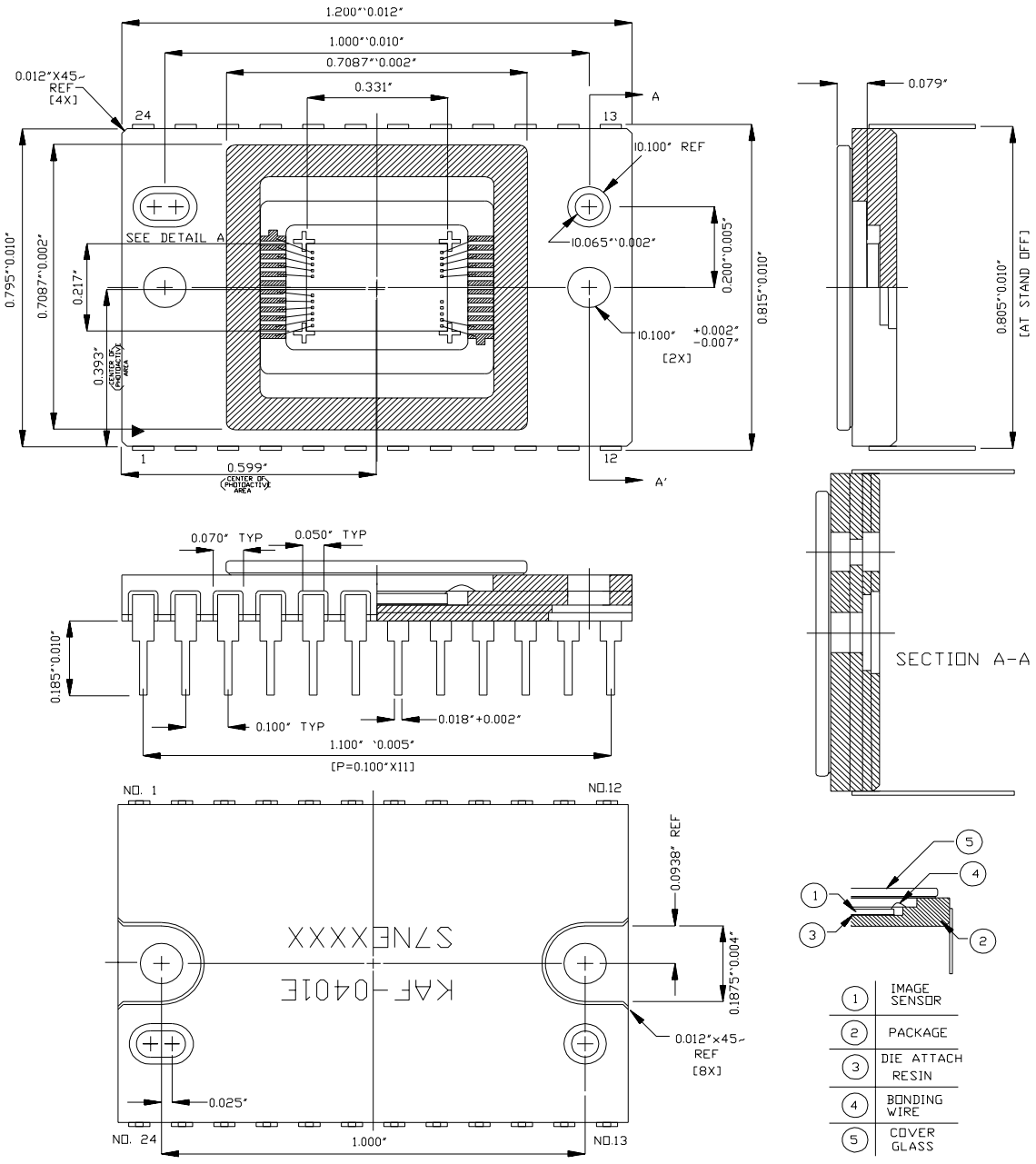


Figure 8 Package dimensions

REVISION CHANGES

Revision Number	Release Date	Description of Changes
A	11/11/02	Initial release; modifications to existing KAF-0402 spec with new format from KAF-1402E spec
B	1/6/03	New spectral response data.
1	1/27/03	First formal release.